Amendments t the Specification:

Please replace the paragraph, beginning at page 1, line 14, with the following rewritten paragraph:

With the development of electronic appliances of higher ~~in~~ performance and smaller in size, there has been an increasing need to improve the packaging density and functions of circuit components. Also with respect to modules incorporating circuit components, there has been a demand for the capability of improving the packaging density and functions. Presently, there is a tendency to form circuit boards in a mutilayer structure in order to mount the circuit components ~~of~~ and improved package density. In particular, a multilayer circuit board using the connection by inner vias has been put to use as a means of increasing the packaging density of a circuit. Further, there has been advanced ~~the~~ development of a component incorporation type of circuit board capable of saving space in terms of mount area and connecting short wiring patterns between LSIs or component parts ~~in the shortest distance is being advanced~~.

Please replace the paragraph, beginning at page 2, line 4, with the following rewritten paragraph:

An example of a process for manufacturing a conventional component incorporation type of circuit board (See Japanese Patent Application Laid-Open Gazette No. 2002-204049. The ~~entire~~ disclosure of the document is incorporated herein by reference in its entirety.) will be described with reference to FIGS. 15 to 23. FIG. 15 is a cross-sectional view of a state in which a mold release layer 10 is formed on the entire area of one surface of a carrier 1 made of copper and a circuit pattern forming material 2 is formed on the mold release layer 10 by electroplating. As a material for the mold release layer 10, Cr, Ti or the like is used. As the circuit pattern forming material 2, copper, tin, zinc, nickel or gold, for example, is used. As shown in FIG. 16, a resist 3 is provided on the circuit pattern forming material 2 and formed into a desired circuit pattern by using a photolithography technique. As shown in FIG. 17, the circuit pattern forming material 2 is formed into a circuit pattern 12 by etching. Thereafter, as shown in FIG. 18, the layer of the resist 3 on the formed circuit pattern 12 is removed.

Please replace the paragraph, beginning at page 3, line 24, with the following rewritten paragraph:

The above-described conventional method of forming the circuit pattern 12 on the carrier 1 by etching, however, necessarily includes the step of first forming the layer of circuit pattern forming material 2 on the carrier 1. The number of process steps is thereby increased, resulting in a reduction in productivity. Moreover, damage ~~even~~ to the carrier 1 ~~is~~ may be caused due to etching variation to considerably reduce the performance of transfer of the circuit pattern into the electrical insulating layer 4, resulting in failure to perform transfer with stability.

Please replace the paragraph, beginning at page 4, line 9, with the following rewritten paragraph:

That is, even if the concentration of the etching solution is made uniform, there is a possibility of the etching solution unnecessarily strongly acting on the circuit pattern 12 ~~unnecessarily strongly~~ due to the density non-uniformity of the circuit pattern 12. In such a case, there occurs not only removal of the circuit pattern forming material 2 to be etched but

also erosion caused by the etching solution of the mold release layer 10 formed between the carrier 1 and the circuit pattern forming material 2 ~~are caused~~. Further, even part of the carrier 1 under the mold release layer 10 may be eroded.